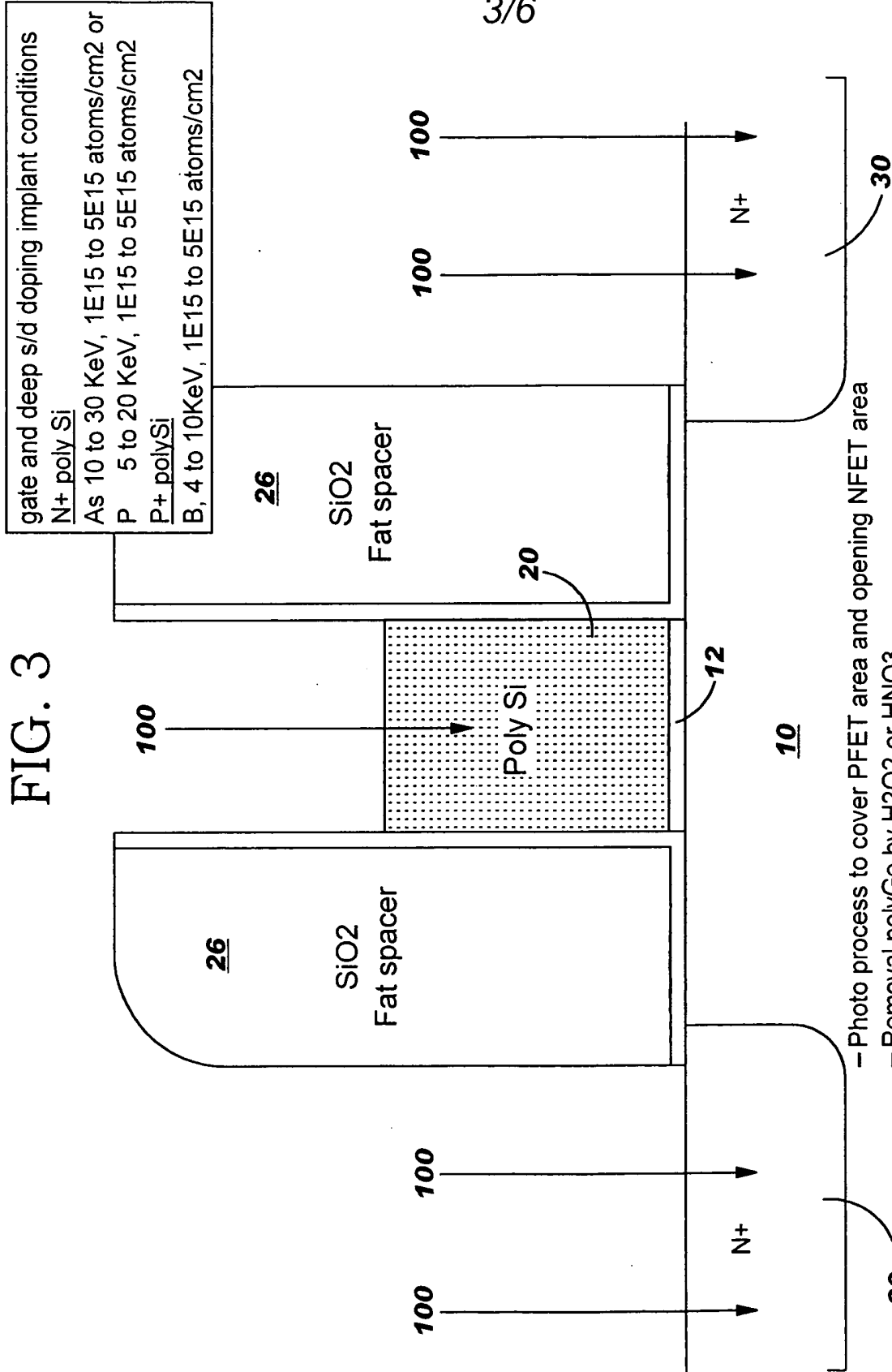


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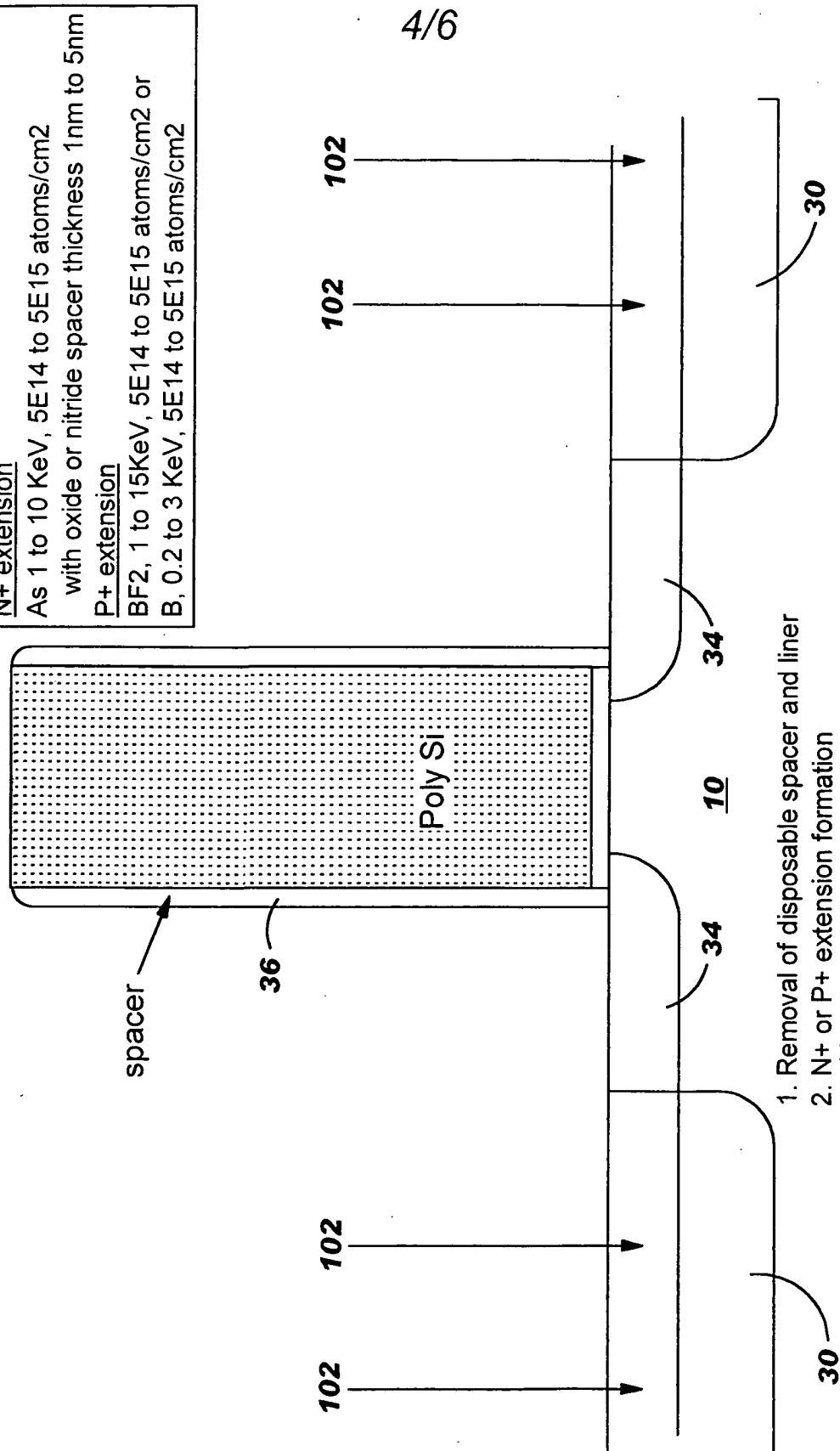
FIG. 3



- Photo process to cover PFET area and opening NFET area
- Removal polyGe by H2O2 or HNO3
- As or P deep implant to dope poly Si and deep n+ s/d
- Photo process to cover NFET area and opening PFET area
- Removal of poly Ge by H2O2 or HNO3
- B deep implant to dope polySi and deep p+ s/d

FIG. 4

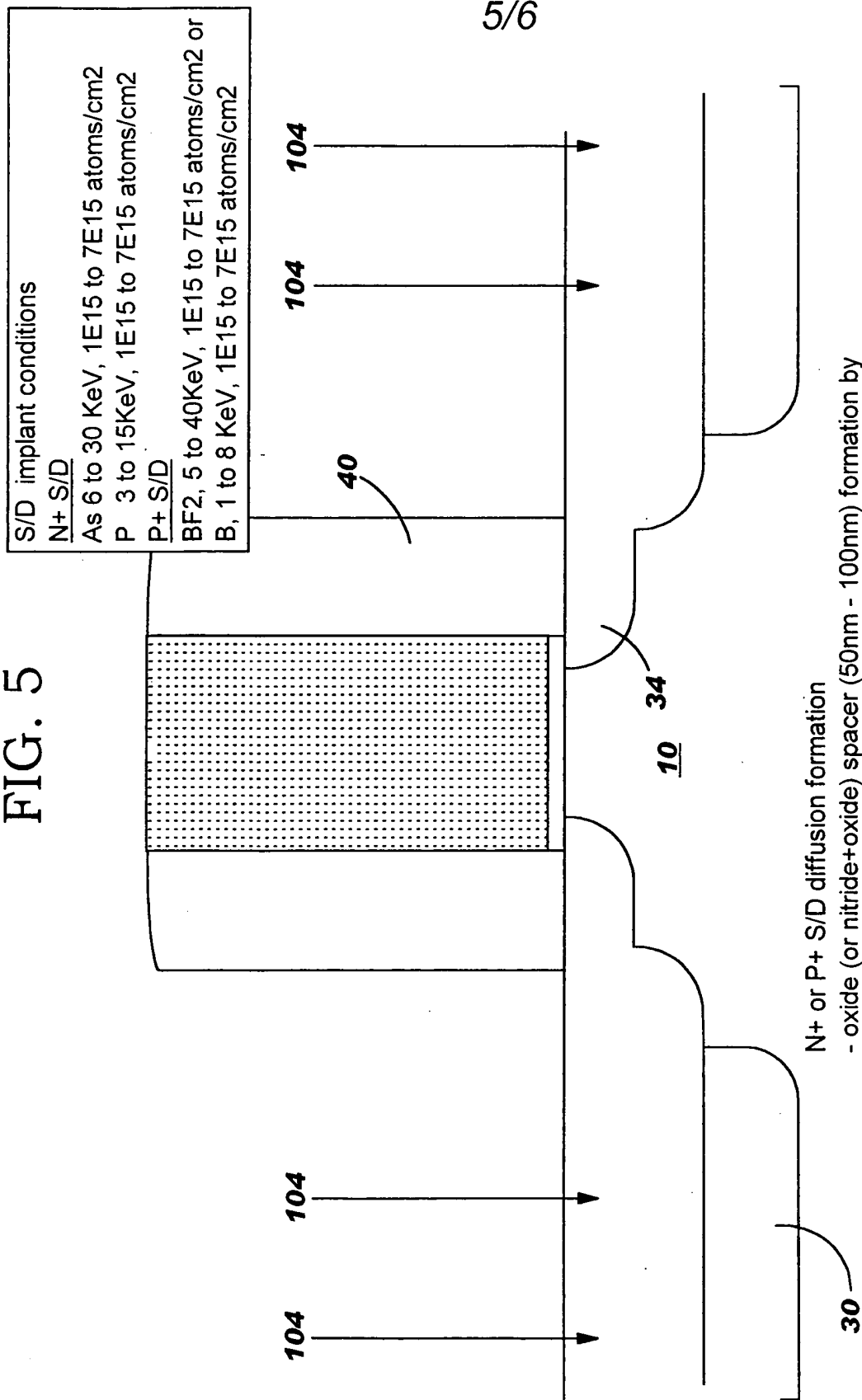
Extension implant conditions	
<u>N+ extension</u>	
As	1 to 10 KeV, 5E14 to 5E15 atoms/cm ²
with oxide or nitride spacer	thickness 1nm to 5nm
<u>P+ extension</u>	
BF ₂	1 to 15KeV, 5E14 to 5E15 atoms/cm ² or
B	0.2 to 3 KeV, 5E14 to 5E15 atoms/cm ²



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1. Removal of disposable spacer and liner
2. N+ or P+ extension formation
 - oxide or nitride spacer (less than 5nm for N, 15nm for P) formation by CVD deposition followed by RIE etch
 - As (for N) or B (for P) ion implantation, (halo implantations if necessary) with appropriate photo process to form implant blocking mask

FIG. 5



N+ or P+ S/D diffusion formation

- oxide (or nitride+oxide) spacer (50nm - 100nm) formation by CVD deposition followed by RIE etch

- As or P (for N+) or B (for P+) ion implantation with appropriate photo process to form implant blocking mask,

- Strip photo resist after the implants

- Dopant activation anneal at 1000C to 1100C, for 10 sec to 10m sec

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